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plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure;

the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefine sectors of a register definition table; and

wherein the computer system further comprises an output means for outputting the register definition file in a manner which is usable to create in silicon the registers of the ASP.

6. A computer system according to claim 5, wherein the input means comprises means for receiving a physical recording device holding the input file for each peripheral.

7. A computer system according to claim 5, wherein the output means comprises means for loading the register definition file onto a physical recording device.

8. A computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer to read an input file which defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language, and to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers.

9. A register definition file stored on a computer readable medium and comprising a plurality of register definition tables, each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word

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9 location of the register within a memory map for access during simulation of an ASP implementing the registers.

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